REMARKS

This responds to the Office Action mailed July 5, 2007 in the present application. The Office Action has been carefully considered. Reconsideration of the application in view of the above claim amendments and following remarks is respectfully requested.

Claim Rejection Under 35 U.S.C. § 112

In the Office Action, claims 1-12 were rejected under 35 U.S.C. § 112, second paragraph, for failing to clearly define the exact structure of the claimed invention. Applicants respectfully submit that claim 1 was amended so as to clearly define the structure and all elements of the claimed power semiconducting device. Reconsideration of claim 1 is respectfully requested.

With respect to the Examiner's observation that the electrically conducing means between the first face and the second ace of the support substrate is not seen in the drawings nor understood as to its structure and geometry. Applicants respectfully submit that the drawings show an embodiment wherein the electrically conducting means of the support substrate is composed of the support substrate itself, which is described at page 8, lines 9-22 of the specification. Accordingly, withdrawal of claim rejections is respectfully requested.

Claim Rejection Under 35 U.S.C. § 103

In the Office Action, claims 1-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,121,661 to Assaderghi, et al. in view of U.S. Patent No. 6,515,332 to Warick. Applicants respectfully traverse.

Assaderghi reference does not render claims of the present application unpatentable either individually or in combination with Warick. First, Assaderghi discloses an SOI structure

for electrostatic discharge (ESD) protection and not to a power semiconductor devices, as claimed in the present application. Second, Assaderghi does not disclose, teach or even suggest electrical connection means, as recited in claim 1 of the present application. For example, careful examination of Fig. 4A of the Assaderghi patent indicates that there is no connection means provided on the rear face of the substrate 42 and there is no mention of such electrical connection anywhere in the specification of the Assaderghi reference.

Furthermore, Applicants disagree with the Examiner's position that "through contact structures are formed to penetrate an epitaxial layer, an insulating layer and the support substrate." First, Assaderghi does not disclose an epitaxial layer. In contrast, Assaderghi only shows a superficial layer of an SOI substrate. Moreover, plugs 48 are not through contact structure but heat paths (see, col. 3, lines 63-67 and col. 4, lines 40-51). At least for these reasons, claim 1 and claims dependent thereon are patentable over Assaderghi reference.

With respect to Warick, Applicants submit that it also fails to render claims of the present application unpatentable either individually or in combination with Assaderghi. First, Warwick relates to an insulated-gate field-effect semiconductor device and not to a power semiconducting device as claimed in the present application. Second, Warwick does not disclose, teach or even suggest an epitaxial layer grown on a transfer layer, as recited in claim 1. At least for these reasons, claim 1 and claims dependent thereon are patentable over Warick reference.

Conclusion

In view of the above, Applicant submit that the present application is in condition for allowance. Favorable disposition to that effect is respectfully requested. If, in the opinion of the

Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

The Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment to Deposit Account No. 50-1698.

Respectfully submitted,

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